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MAC/PHY INTERFACE

5 The invention is related to and claims priority under 35 USC 119(e)(1) from the following co-pending U.S. Provisional Patent Applications: serial number 60/172,516 by Lu et al., entitled A Programmable Multi-standard MAC Architecture, and filed on December 17, 1999; and serial number 60/172,541 by Lu et al., entitled DSP Core/PHY Interface Specification, and filed on December 17, 1999. In addition, the invention is related to the simultaneously filed co-pending U.S. Patent Application serial number 09/737,714 (docket number 10 TI-30142), entitled A Programmable Multi-Standard MAC Architecture, by Lu et al.. All of the aforementioned patent applications are hereby incorporated by reference.

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